

ABSTRACT

An insertion sorter circuit and method are provided which are particularly useful for sorting channel response values of a communication signal. The sorter circuit includes a series of sorter elements which each have a register. The circuit is configured to cascade values downwardly when one register receives a greater value than it has stored, which value is not greater than the value stored in any upstream register. At the end of processing the values, the most significant values are stored in the registers, the sum of which are the channel power estimate. The channel noise variance is obtainable by applying a system dependent scaling factor to the sum of the least significant values processed.